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(19)



Europäisches Patentamt
European Patent Office
Office européen des brevets



(11) Publication number:

0 609 867 A2

(12)

EUROPEAN PATENT APPLICATION

(21) Application number: **94101571.1**

(51) Int. Cl.⁵: **H01L 21/20, H01L 21/336**

(22) Date of filing: **02.02.94**

(30) Priority: **03.02.93 JP 39499/93**

(43) Date of publication of application:
10.08.94 Bulletin 94/32

(84) Designated Contracting States:
DE FR GB NL

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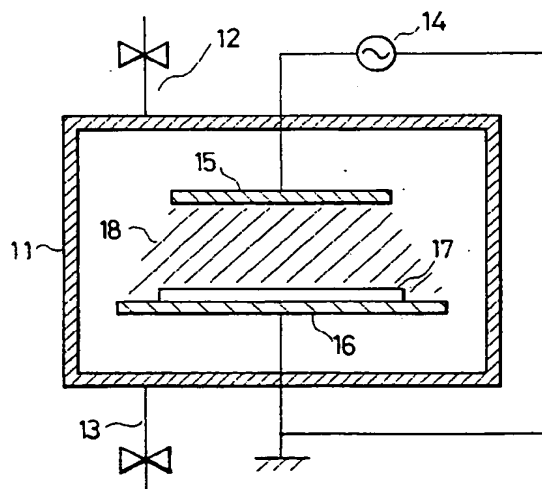
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(54) **Process for fabricating a semiconductor crystallized layer and process for fabricating a semiconductor device using the same.**

(57) A process for fabricating a semiconductor at a lower crystallization temperature and yet at a shorter period of time, which comprises forming an insulator coating on a substrate; exposing said insulator coating to a plasma; forming an amorphous silicon film on said insulator coating after its exposure to said plasma; and heat treating said silicon film in the temperature range of from 400 to 650 °C or at a temperature not higher than the glass transition temperature of the substrate. The nucleation sites are controlled by selectively exposing the amorphous silicon film to a plasma or by selectively applying a substance containing elements having a catalytic effect thereto. A process for fabricating a thin film transistor using the same is also disclosed.

FIG. 1



EP 0 609 867 A2

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BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates to a process for fabricating a crystalline semiconductor for use in thin film devices such as thin-film insulated-gate field-effect transistors (hereinafter referred to simply as "thin film transistors" or "TFTs"). The present invention also relates to a process for fabricating a semiconductor device using the same.

2. Prior Art

Thin films of crystalline silicon semiconductor for use in thin film devices such as TFTs known heretofore have been fabricated by crystallizing an amorphous silicon film formed through plasma CVD (chemical vapor deposition) or thermal CVD, using an apparatus such as an electric furnace maintained at a temperature of not lower than 600 °C for a duration of 12 hours or longer. Thin films of crystalline silicon semiconductor having sufficiently high quality (for example, an excellent field effect and a high reliability) are available only after subjecting the amorphous film to a heat treatment for a still longer duration.

However, those prior art processes for obtaining thin films of crystalline silicon semiconductor suffer various problems yet to be solved. One of the problems is the low throughput which increases the process cost. For instance, if a duration of 24 hours is required for the crystallization step, 720 substrates must be processed at a time considering that preferably, the substrates each consume 2 minutes of process time. However, the maximum number of substrates an ordinary tubular furnace can treat at a time is limited to 50; in a practical treatment using only one apparatus (reaction tube), it has been found that a single substrate consumes 30 minutes to complete the treatment. In other words, at least 15 reaction tubes are necessary to complete the reaction per single substrate in 2 minutes. This signifies an increase in investment cost and therefore an increase of the product price due to a too large depreciation for the investment.

The temperature of the heat treatment is another problem to be considered. In general, a TFT is fabricated using a quartz glass substrate comprising pure silicon oxide or an alkali-free borosilicate glass substrate such as the #7059 glass substrate manufactured by Corning Incorporated (hereinafter referred to simply as "Corning #7059 substrate"). The former substrate has such an excellent heat resistance that it can be treated in the same manner as in a conventional wafer process for semiconductor integrated circuits. However, it is expensive, and, moreover, the price

increases exponentially with increasing the area of the substrate. Thus, at present, the use of quartz glass substrates is limited to TFT integrated circuits having a relatively small area.

On the other hand, alkali-free borosilicate glass substrates are inexpensive as compared to those made of quartz glass, however, they have shortcomings with respect to their heat resistance. Since an alkali-free glass substrate undergoes deformation at a temperature in the range of from 550 to 650 °C and more particularly, since a readily available material initiates its deformation at a temperature higher than 600 °C, any heat treatment at 600 °C causes an irreversible shrinkage and warping to form on the substrate. These deformations appear particularly distinctly on a substrate having a diagonal length of more than 10 inches. Accordingly it is believed requisite to perform the heat treatment on a silicon semiconductor film at a temperature of 550 °C or lower and for a duration of within 4 hours to reduce the entire process cost.

SUMMARY OF THE INVENTION

In the light of the aforementioned circumstances, an object of the present invention is to provide a process for fabricating a semiconductor which can resist to a heat treatment conducted under the above conditions, and to provide a process for fabrication a semiconductor device using such semiconductors.

An embodiment according to the present invention provides a process for fabricating a semiconductor which is characterized in that it comprises forming an insulator coating on a substrate; exposing said insulator coating to a plasma; forming an amorphous silicon film on said insulator coating after its exposure to said plasma; and crystallizing said silicon film by photo annealing said silicon film and/or heat treating said silicon film in the temperature range of from 400 to 650 °C or at a temperature not higher than the glass transition temperature of the substrate.

Another embodiment according to the present invention provides a process for fabricating a semiconductor which is characterized in that it comprises forming an insulator coating on a substrate; selectively coating said insulator film with a masking material; exposing said substrate to a plasma; forming an amorphous silicon film on said insulator coating after exposing the substrate to said plasma; crystallizing said silicon film by photo annealing said silicon film and/or heat treating said silicon film in the temperature range of from 400 to 650 °C or at a temperature not higher than the glass transition temperature of the substrate; and selectively etching said silicon film.

Furthermore, still another embodiment according to the present invention comprises fabricating a thin film transistor which is characterized in that it comprises forming an insulator coating on a substrate; selectively coating said insulator coating with a masking material; exposing said substrate to a plasma; forming an amorphous silicon film on said insulator coating after exposing the substrate to said plasma; crystallizing said silicon film by photo annealing said silicon film and/or heat treating said silicon film in the temperature range of from 400 to 650 °C or at a temperature not higher than the glass transition temperature of the substrate; selectively etching said silicon film; and establishing a channel forming region of a thin film transistor from the portion previously coated with the masking material.

Yet another embodiment according to the present invention provides a process for fabricating a semiconductor, which is characterized in that it comprises forming an amorphous silicon film on a substrate; forming, in intimate contact with the upper or the lower surface of said silicon film, a substance comprising an element which accelerates the crystallization of amorphous silicon by exerting a catalytic effect thereto; and crystallizing the silicon film by photo annealing the silicon film and/or heating the silicon film in the temperature range of from 400 to 650 °C or at a temperature not higher than the glass transition temperature of the substrate. More specifically, the present process is accomplished by coating the surface of a base coating of the amorphous film with a solution containing water, an alcohol (either monohydric or polyhydric), a petroleum solvent (which may be a saturated or an unsaturated hydrocarbon), and the like, dissolved or dispersed therein an acetate or a nitrate, any type of carboxylate, or any other organic acid salt of an element which accelerates the crystallization. The coating may be otherwise provided on the upper surface of the amorphous coating film. The resulting amorphous coating is then subjected to heat treatment.

Still another embodiment according to the present invention provides a process for fabrication a semiconductor, characterized in that it comprises forming an insulator coating on a substrate; selectively coating said insulator coating with a masking material; exposing said substrate to a plasma or forming a coating of a substance containing an element which has a catalytic effect and accelerates the crystallization of the amorphous silicon; forming an amorphous silicon film on said insulator coating after subjecting the substrate to said previous step; crystallizing said silicon film by photo annealing said silicon film and/or heat treating said silicon film in the temperature range of from 400 to 650 °C or at a temperature not higher than the

glass transition temperature of the substrate; and selectively etching said silicon film.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 shows a schematic view of an apparatus for performing a process according to an embodiment of the present invention (see Example 1);

FIGs. 2(A) to 2(C) show schematically drawn step sequential cross section structures obtained in a process according to an embodiment of the present invention, in which selective crystallization is employed (Example 2);

FIGs. 3(A) to 3(E) show schematically drawn step sequential cross section structures obtained in a process for fabricating a TFT according to an embodiment of the present invention (Example 3);

FIGs. 4(A) to 4(F) show schematically drawn step sequential cross section structures obtained in another process for fabricating a TFT according to an embodiment of the present invention (Example 3);

FIG. 5 shows a schematic view of an apparatus for performing a process according to an embodiment of the present invention (see Example 1);

FIG. 6 shows the change of Raman scattering intensity ratio with the duration of annealing observed on a silicon film obtained in Example 1, in which the intensity ratio signifies the relative intensity taking the Raman scattering intensity of a standard sample (single crystal silicon) as unity;

FIG. 7 shows the change of Raman scattering intensity ratio with changing temperature of annealing observed on a silicon film obtained in Example 1, in which the intensity ratio signifies the relative intensity taking the Raman scattering intensity of a standard sample (single crystal silicon) as unity;

FIGs. 8(A) to 8(D) show schematically drawn step sequential cross section structures obtained in still another process for fabrication a TFT according to an embodiment of the present invention (Example 8);

FIGs. 9(A) to 9(E) show schematically drawn step sequential cross section structures obtained in yet another process for fabricating a TFT according to an embodiment of the present invention (Example 9); and

FIG. 10 shows the nickel concentration in silicon crystal.

DETAILED DESCRIPTION OF THE INVENTION

After an extensive study, the present inventors have found a means for overcoming the aforementioned problems. More specifically, the present inventors formed a lower insulator layer on a substrate to prevent impurities from intruding into the semiconductor layer from the substrate, and, after once exposing the insulator layer to plasma, deposited a layer of amorphous silicon and optically and/or thermally crystallized the amorphous silicon. Thus, it has been found that a silicon semiconductor film deposited on the resulting structure can be crystallized considerably easily.

The aforementioned findings can be explained as follows. The reason why a conventional thermal crystallization process at about 600 °C requires a long period of time can be explained, in one aspect, by the generation of crystal nuclei which takes a long time. In the present specification, this period of time is referred to as a latent period. According to the 24-hour observation of a crystallization process by the present inventors, silicon maintains its initial amorphous state in the initial period of six hours because no nucleus is formed during this period. In the subsequent period of six hours, nuclei are generated spontaneously, and this step is followed by the crystallization. It can be seen that a prior art process includes a latent period for a duration of from 6 to 12 hours in the entire process time. However, the nuclei thus formed during the latent period are highly disorder, and the concentration of the nuclei differs from a place to place. Thus, in particular regions, it happens that the crystallization greatly proceeds; but in other regions, substantially no crystallization is observed to occur. However, with passage of time, nucleation occurs also in those regions in which no nucleation had been observed, or the region of crystallization extends to gradually cover the entire substrate. It can be seen that a period of 12 hours or longer is necessary to obtain a completely crystallized substrate.

When the base insulator film is treated with a plasma, a substance which functions as a catalyst for accelerating the crystallization is formed in the insulator film. A catalyst which accelerates the nucleation signifies, for example, a charge or a defect which results from the damage caused by the plasma, or a deposit from a material which constitutes the chamber or the substrate. More specifically, those from materials having a catalytic effect on crystallization, such as nickel, iron, cobalt, and platinum, are found to have marked effects as catalysts. The presence of these catalysts facilitates nucleation and shortens the latent period. Moreover, a larger number of crystal nuclei can be obtained by increasing the amount of these cata-

lysts. This can be assumed by the fact that a longer plasma treatment allows nucleation to occur at a higher density and that it leads to the generation of finer crystals.

Another aspect to be noticed in the plasma treatment is that the nucleation occurs in an extremely uniform density over the entire substrate. This can be confirmed by observing the lightly etched surface of a silicon film crystallized by the present invention. More specifically, the surface of a specimen obtained by depositing an amorphous silicon film on a plasma-treated substrate and thermally treating the resulting structure at 550 °C for a duration of 4 hours is observed under an optical microscope, electron microscope, and the like after lightly etching the surface using a fluoronitric acid. Then, it can be found that crater-like minute holes are formed at approximately the same spacing. These holes are believed attributable to the presence of materials liable to be readily etched. In other words, the etched pattern corresponds to the density distribution of crystal nuclei inside the silicon film. It can be assumed that the catalyst is distributed in the same manner as the density distribution pattern of the holes. In the process according to the present invention, a preferred nickel concentration is in the range of from 1×10^{15} atoms·cm⁻³ to 1 % by atomic, and more preferably, the nickel concentration is in the range of from 1×10^{16} atoms·cm⁻³ to 0.001 % by atomic. Most preferably, the minimum concentration is in the range of from 1×10^{15} to 1×10^{17} atoms·cm⁻³ as observed by SIMS (secondary ion mass spectrometer). If the nickel concentration exceeds the above value, the characteristics of the resulting semiconductor would be greatly impaired. On the other hand, if the nickel concentration should fall lower than the defined range, no crystallization proceeds at a temperature of 590 °C or lower.

Favorable results on the plasma treatment can be obtained by performing the treatment using a parallel-plate type plasma generation apparatus. Otherwise, the use of a positive column discharge in a chamber while applying a proper bias can also yield favorable results. At any rate, preferred results can be obtained by using an electrode made of nickel, iron, or cobalt for generating the plasma.

Furthermore, the crystallization occurs more easily by heating the substrate to a temperature range of from 100 to 500 °C during the plasma treatment, and more specifically, the substrate is preferably heated to a temperature of 200 °C or higher. This is because the catalytic substance can be more readily obtained at higher temperatures.

Best results on plasma treatment can be obtained by generating the plasma in an atmosphere containing nitrogen, oxygen, argon, neon, or krypton, and particularly, when these gases are con-

tained in an amount of 10 volume by % or more. The gas is preferable diluted using hydrogen or helium. Moreover, the silicon films which yield the best results were found to be intrinsic or substantially intrinsic, and they were found to contain the foreign elements carbon, oxygen, and nitrogen each at a concentration of $1 \times 10^{19} \text{ cm}^{-3}$ or lower by SIMS (secondary ion mass spectroscopy).

The process according to the present invention comprises plasma treating the surface of a base insulator film. However, when a substrate once subjected to plasma treatment is exposed to the atmosphere, dust, water, and other impurities adhere to the surface to greatly impair the crystallinity of the silicon film. In other words, substrates having a non-uniform characteristics result by the exposure of the substrate to the atmosphere. Such a problem can be circumvented by performing the film deposition and the plasma treatment in a closed system, and maintaining an environment in which the film deposition can be performed continuously without exposing the plasma-treated substrate to air. Furthermore, preferably, the surface of the substrate and the insulating coating is maintained at a sufficiently clean state. For instance, carbon, organic matter, and the like are preferably removed from the surface by employing ultraviolet irradiation, ozone treatment, or a combination thereof.

The present inventors further extended the study above, and thought of a simple process which comprises applying a substance containing an element capable of accelerating the crystallization or a compound thereof to achieve similar results as those obtained by plasma treating the surface of the insulator coating. By using such a means, the conventional installation can be used as it is without additionally furnishing it with a vacuum apparatus. In the use of such substance, however, it has been feared that oxygen and carbon included in the salt may diffuse into the silicon film and that they may degrade the semiconductor characteristics of the silicon film. Accordingly, the present inventors conducted a study using thermogravimetry and differential thermal analysis to find that, by properly selecting the material, such additional substances decompose to yield oxides or elements at a temperature of 450°C or lower, and that no further diffusion of such substances occurs to allow them penetrate into the silicon film. In particular, when decomposed under a reducing atmosphere such as nitrogen gas, salts such as acetates and nitrates were found to yield elemental metal at a temperature of 400°C or lower. These salts yield oxides at first through decomposition in an oxygen atmosphere, but they finally yield elemental metal at higher temperatures upon the desorption of oxygen.

After thus introducing an element which accelerates the crystallization of at least a part of the silicon film, the entire structure was subjected to annealing in the temperature range of from 400 to 650°C . Similar to the foregoing process which comprises applying a plasma treatment, crystallization was found to occur on the amorphous silicon film after the passage of 2 hours.

However, the catalytic elements above, i.e., nickel, iron, cobalt, and platinum themselves are not favorable for silicon. Accordingly, their concentration is preferable suppressed as low as possible. The present inventors have found, through an extensive study, that the concentration of these elements for a semiconductor to be used in a semiconductor device such as a TFT is preferable controlled, from the viewpoint of assuring favorable characteristics and reliability, to be in the range of from $1 \times 10^{15} \text{ atoms}\cdot\text{cm}^{-3}$ to 1 atom%, and more preferably, in the range of from $1 \times 10^{16} \text{ atoms}\cdot\text{cm}^{-3}$ to 0.001 atom%. Most preferable, the minimum concentration of the catalytic metal elements is in the range of from 1×10^{15} to $1 \times 10^{19} \text{ atoms}\cdot\text{cm}^{-3}$ as observed by SIMS (secondary ion mass spectrometer). If the concentration of the catalytic metal elements should fall below this range, sufficient crystallization would not result. If the concentration should exceed this range, on the other hand, semiconductors with poor characteristics and reliability would be obtained.

The present invention is illustrated in greater detail referring to non-limiting examples below. It should be understood, however, that the present invention is not to be construed as being limited thereto.

EXAMPLE 1

A process for crystallizing a planar amorphous silicon film formed on a Corning #7059 substrate is described below. A $2,000 \text{ \AA}$ thick silicon oxide film was deposited on the substrate as a base film using RF sputtering, and the resulting silicon oxide film was treated in nitrogen plasma. A plasma treating apparatus was of a parallel plane type as shown schematically in FIG. 1. It comprises a chamber 11, a gas inlet system 12, an evacuation system 13, an RF power source 14, and nickel-alloy electrodes 15 and 16, so that the substrate 17 may be placed under an RF plasma 18.

The plasma treatment was performed for a duration of 5 minutes by applying an RF power of 20 W or 60 W under a reaction pressure of 10 Pa (where, a vacuum degree of 10^{-3} Pa or lower is achieved), while flowing nitrogen as the reactive gas at a flow rate of 100 SCCM (standard cubic centimeters per minute) and setting the substrate temperature to 200°C .

Then, a 1,500 Å thick amorphous silicon film was deposited by plasma CVD, and after removing hydrogen from the film by keeping it at a temperature of 430 °C for 1 hour, solid phase growth was allowed to take place thereon in the temperature range of from 500 to 580 °C for a duration of from 10 minutes to 8 hours. The solid phase growth may be carried out by irradiating a laser light thereto before or after or at the same time as heating in the above temperature range.

The above steps may be performed otherwise using, for example, an apparatus having two or more chambers as shown in FIG. 5, so that the steps can be performed continuously. Particularly, the above processes comprise depositing the amorphous silicon film after once exposing the plasma-treated silicon oxide base to air. The process according to the present invention is sensitive to the surface conditions, and the characteristics of the resulting crystalline silicon film tend to be greatly influenced by the inclusions which may adhere to the surface of the substrate during its exposure to air.

Referring briefly to the apparatus illustrated in FIG. 5, it comprises a chamber 501 which is a sputtering apparatus, and a plasma is generated by supplying electric power to two electrodes (sample holder and a backing plate) 502 and 503 from an RF power source 504. A substrate 506, which is the sample, and a target 505 are placed on the respective electrodes. The target 505 in this case is silicon oxide. The chamber 501 is further equipped with a gas system 507 for introducing a gas mixture comprising oxygen gas and argon gas, and another gas system 508 for introducing nitrogen gas. Thus, a gas is supplied from the former system during the deposition of the film, and during the plasma treatment, the gas is supplied from the latter system. An evacuation system 509 is also provided to the chamber 501.

The apparatus further comprises a chamber 521 which is a plasma CVD apparatus of a parallel plane type. A plasma can be generated inside the chamber 521 by supplying an electric power from a power source 524 to two electrodes 522 and 523 provided inside the chamber 521. A sample substrate 525 is mounted on the electrode 522 so that a coating which generates by a plasma reaction would form on the substrate upon introducing a gas mixture of silane and hydrogen into the chamber through a gas system 526. Though not shown in the figure, a mechanism is provided to those chambers as such that the substrate can be heated to a proper temperature.

An additional chamber 510, in which a substrate 511 is placed, is provided between the two plasma chambers.

In a process using the apparatus illustrated in FIG. 5, nitrogen plasma treatment is performed immediately after the completion of silicon oxide film deposition using sputtering in the chamber 501, by replacing the atmosphere inside the chamber with nitrogen. If a silicon oxide target should remain inside the chamber, further deposition of silicon oxide film occurs by sputtering. To prevent this from occurring, the RF power must be lowered or the silicon oxide target must be isolated from the plasma. Fortunately, as described hereinafter, plasma treatment is performed optimally at a power of 60 W or lower, and preferably, at a power of 20 W, as compared to an RF power of 100 W or higher required for sputtering. Accordingly, no deposition of silicon oxide occurred during the treatment in nitrogen plasma. To further assure the process, however, a chamber for depositing the silicon oxide film is preferably installed separately from the chamber for use in plasma treatment. An amorphous silicon film thus deposited was also subjected to solid-phase crystallization under the same conditions described hereinbefore.

After allowing the amorphous silicon film to undergo solid phase crystal growth, the degree of crystallization thereof was evaluated using Ar⁺-laser Raman spectroscopy. The results are shown in FIGs. 6 and 7. The ordinate in both of the graphs represents relative intensity taking the Raman peak intensity of a standard sample (a single crystal silicon) as unity. It can be read from the graphs that no crystallization occurs by heat treating a sample without plasma treatment at 580 °C or lower for a duration of 8 hours or less. In contrast to this, both of the samples plasma-treated at an RF power of 20 W and 60 W are found to undergo crystallization.

With a careful inspection of the results, it can be seen that the crystallization proceeds as a function of the RF power applied at the plasma treatment. More specifically, the crystallization proceeds rather sluggishly when plasma treatment is performed under a low power of 20 W. At least an annealing for a duration of 1 hour is necessary to crystallize the amorphous silicon film at 550 °C. In other words, the latent period in this case is 1 hour. However, after the passage of an hour, the crystallization proceeds swiftly to attain a saturated state within 2 hours of annealing. By comparing the Raman peak intensity, it can be seen that a crystallization degree well comparable to that of a standard sample, i.e., a single crystal silicon, is achieved for the sample after the annealing of 2 hours.

In contrast to the case above, crystallization proceeds relatively swiftly in the case a high RF power of 60 W is applied at the plasma treatment. For example, an annealing for 4 hours allows the

amorphous silicon film to crystallize at a temperature as low as 480 °C, and by increasing the temperature to 550 °C, an annealing for a duration of mere 10 minutes (i.e., a latent period of 10 minutes) initiates crystallization and achieves a saturated state in an hour. However, the degree of crystallization is low, and by comparing the Raman intensity, it can be seen that the degree of crystallization achieved in this case only corresponds to less than 70 % of that obtained for a silicon film crystallized under a low power of 20 W.

This difference can be explained in terms of the nucleation density. That is, nuclei generate at a low density when the plasma treatment is applied under a low power condition, because the concentration of the catalytic substance is low. Thus, the crystallization of these nuclei requires a treatment at a high temperature and a long duration. However, the resulting crystallites have high crystallinity and yield a high Raman intensity ratio. On the other hand, catalytic substances are generated at a high concentration by applying a plasma treatment under a condition of high power. Since nucleation occurs at high nuclei interfere each other during their growth, and the film which is obtained as a result has a poor crystallinity.

At any rate, the application of a plasma treatment enables crystallization to take place at a low temperature and within a short period of time as compared to the case with no plasma treatment. Obviously, the crystallization at a low temperature and in a short period of time is achieved by applying a plasma treatment. In the present example, the concentration of the catalytic substance was controlled by controlling the RF power, however, other factors, such as the pressure applied during the plasma treatment, the type and the component of gas, the temperature of the sample, and the duration of processing, are all important factors for controlling the concentration of the catalytic substance.

EXAMPLE 2

A process for selectively crystallizing an amorphous silicon film by selectively treating the oxide film base using a plasma treatment is described below. Referring to FIG. 2, a 2,000 Å thick silicon oxide film 22 was deposited as a base on a Corning #7059 substrate 21 by sputtering, and a heat-resistant photoresist 24 was applied thereon by spin-coating. After patterning the resulting photoresist film 24, the entire substrate was exposed to nitrogen plasma in the same manner as in Example 1 to perform plasma treatment on the exposed portion 23 of the oxide film base. The plasma treatment was effected under the same conditions as those employed in Example 1, except

for setting the RF power to 60 W. Thus was obtained a structure shown in FIG. 2(A).

Since the substrate at this point is heated to a temperature of 200 °C or higher, the masking material to be used herein must at least resist to the same temperature. Furthermore, preferably, the masking material is removable without using a plasma. Thus, the use of a heat-resistant photoresist for the mask is preferred from these points of view. Otherwise, inorganic materials such as titanium nitride, silicon oxide, and silicon nitride can be used as well.

Subsequently, an annealing at 550 °C for a duration of 4 hours is performed after depositing a 1,500 Å thick amorphous silicon film 25 by low pressure CVD. As a result, crystalline silicon 26 was observed to form around the portions remained uncovered by the masking material on plasma treatment. The crystallization extended into portions covered by the masking material (but only portions treated by the plasma) for about 5 μm along the longitudinal direction. No crystallization was observed to occur on other portions covered by the masking material. The annealing may be carried out by irradiating a laser light thereto before or after or at the same time as heating at 550 °C as described above.

Noticeably, the crystallinity for the portions subjected to plasma treatment were lower than that of the peripheral portions at a distance of 5 μm from those plasma-treated portions. In the portions directly subjected to plasma treatment, the fact is that the crystallites initiate growth from a plurality of independent nuclei, and that then they collide with each other to interfere their growth. On the other hand, the peripheral portions contain no nucleus, and the direction of crystal growth is confined to a single direction. It can be seen that the crystal growth is allowed to take place without any limitations.

EXAMPLE 3

A process for fabricating a TFT having particularly high mobility by selectively performing a plasma treatment is described below. More specifically, the masking material was formed only on a portion for fabricating a channel forming region (i.e., a region located under the gate contact and between a source and a drain in an island-like semiconductor region) of a TFT to prevent this portion from being exposed to plasma. However, since crystallization proceeds, though depending on the annealing temperature and duration, in a region from several micrometers to ten micrometers in size as described in the foregoing EXAMPLE 2, this process is not suitable for a device having too long a channel length and too wide a channel width.

In the plasma treatment, the surface of the silicon oxide base is subject to defects due to the impact exerted by the plasma. Moreover, various types of foreign matter adhere to the surface. A part of these defects and foreign matter functions as a catalyst to accelerate nucleation, however, it also may cause leak current if it is found in the channel forming region of a TFT. Furthermore, a TFT having high mobility can be obtained only by using semiconductors of high crystallinity. Thus, by referring to EXAMPLE 2 above, the peripheral portions are preferred to the plasma treated portions in this case.

Referring to FIG. 3, the process according to the present example is described below. A 2,000 Å thick silicon oxide film 31 was deposited as a base on a Corning #7059 substrate 30 by sputtering, and a heat-resistant photoresist was applied thereon to form masks 32A and 32B each at the same size as the channel, i.e., 5 μm x 15 μm. Otherwise, the mask can be patterned using the patterning for the gate connection, because, as described hereinafter, the effect is the same for both considering that the crystallization is effected after patterning the amorphous silicon film. The resulting substrate was placed into a plasma 33 to perform the plasma treatment as shown in FIG. 3(A). The same plasma treating apparatus as that used in EXAMPLE 1 was used. The plasma treatment was performed for a duration of 5 minutes by applying an RF power of 60 W under a reaction pressure of 10 Pa (where, a vacuum degree of 10^{-3} Pa or lower is achieved), while flowing nitrogen as the reactive gas at a flow rate of 100 SCCM (standard cubic centimeters per minute) and maintaining the substrate temperature to 200 °C.

The masks 32A and 32B were removed after the plasma treatment, and a 1,500 Å thick amorphous silicon film was deposited thereon by low pressure CVD using monosilane (SiH_4) as the material gas. Subsequently, annealing was effected at 550 °C for a duration of 4 hours to allow the film to crystallize. A laser light may be irradiated to the film for crystallization of the film before or after or at the same time as the annealing. The thus crystallized film was patterned to form island-like silicon regions 34A and 34B, and this was followed by the deposition of a 1,000 Å thick silicon oxide film 35 by plasma CVD using tetraethoxysilane (TEOS) and oxygen as the material gases. After depositing an N-type polysilicon film by low pressure CVD, the resulting structure was subjected to patterning to form a gate connection with gate contact 36A and 36B. The resulting structure is shown in FIG. 3(B).

Then, impurities were introduced using plasma doping. In this case, phosphine (PH_3) gas and diborane (B_2H_6) gas were used as the N-type and

P-type impurity sources, respectively. Phosphine was doped by applying an accelerating voltage of 80 keV, and diborane was doped under a voltage of 65 keV. The impurity region 37 was formed by further annealing the structure at 550 °C for 4 hours to activate the impurities. The activation of the impurities can be performed by a method using an optical energy, such as laser annealing and flash lamp annealing. The resulting structure is shown in FIG. 3(C).

Finally, a 5,000 Å thick silicon oxide film was deposited as an interlayer insulator 38 in the same manner as in an ordinary process for fabricating a TFT. By forming contact holes in the resulting silicon oxide film, connection and contacts 39A and 39B were formed in the source region and the drain region. Thus was obtained the final structure of the TFT as shown in FIG. 3(D).

The final structure of the TFT circuit as viewed from the upper side is given in FIG. 3(E). The cross section views in FIGs. 3(A) to 3(D) are taken along the dashed line drawn in FIG. 3(E). The TFT thus obtained was found to have a field-effect mobility of from 40 to 60 cm^2/Vs in the N-channel type, and of from 30 to 50 cm^2/Vs in the P-channel type.

EXAMPLE 4

A process for fabricating an aluminum-gate TFT according to the present invention is described below.

Referring to FIG. 4, a 2,000 Å thick silicon oxide film 41 was deposited as a base on a Corning #7059 substrate 40 by sputtering, and the entire substrate was exposed to plasma 42 as shown in FIG. 4(A) to effect the plasma treatment. The same plasma treatment apparatus as that used in EXAMPLE 1 was employed. The plasma treatment was performed for a duration of 5 minutes by applying an RF power of 60 W under a reaction pressure of 10 Pa (where, a vacuum degree of 10^{-3} Pa or lower is achieved), while flowing argon as the reactive gas at a flow rate of 100 SCCM (standard cubic centimeters per minute) and maintaining the substrate temperature to 200 °C.

Then, a 1,500 Å thick amorphous silicon film 43 was deposited thereon by low pressure CVD using monosilane (SiH_4) as the material gas. Subsequently, annealing was effected at 550 °C for a duration of 4 hours to allow the film to crystallize. A laser light may be irradiated to the film for the crystallization of the film before or after or at the same time as the annealing. The resulting structure is shown in FIG. 4(B).

The thus crystallized film was patterned to form an island-like silicon region 44, and this was followed by the deposition of a 1,000 Å thick silicon oxide film 45 by plasma CVD using tetraethox-

ysilane (TEOS) and oxygen as the material gases. After depositing a 5,000 Å thick aluminum film containing 1 % of silicon by sputtering, the aluminum film was patterned to form a gate connection and contact 46. The resulting structure is shown in FIG. 4(C).

Subsequently, the entire substrate was subjected to anodic oxidation by dipping it into an ethylene glycol solution containing 3 % of tartaric acid and applying current between a platinum cathode and the aluminum connection 46 (anode). The current was applied in such a manner that the voltage thereof would increase in the initial state at a rate of 2 V/minute, and that a constant voltage is maintained after a voltage of 220 V is attained. The current was turned off at the point the current dropped to 10 $\mu\text{A}/\text{m}^2$ or lower. Thus was obtained a 2,000 Å thick anodic oxide 47 as shown in FIG. 4(D).

Then, impurities were introduced using plasma doping. In this case, phosphine (PH_3) gas and diborane (B_2H_6) gas were used as the N-type and P-type impurity sources, respectively. Phosphine was doped by applying an accelerating voltage of 80 keV, and diborane was doped under a voltage of 65 keV. The impurity region 48 was formed by further laser annealing the structure applying 5 shots using a KrF excimer laser operating at a wavelength of 248 nm and emitting a laser beam at an energy density of from 250 to 300 mJ/cm^2 . The resulting structure is shown in FIG. 4(E).

Finally, a 5,000 Å thick silicon oxide film was deposited as an interlayer insulator 49 in the same manner as in an ordinary process for fabricating a TFT. By forming contact holes in the resulting silicon oxide film, connection and contacts 50A and 50B were formed in the source region and the drain region. Thus was obtained the final structure of the TFT as shown in FIG. 4(F).

The TFT thus obtained was found to have a field-effect mobility of from 40 to 60 cm^2/Vs in the N-channel type, and of from 30 to 50 cm^2/Vs in the P-channel type. Furthermore, a shift resistor fabricated using this TFT was observed to operate at 6 MHz with a drain voltage of 17 V, and at 11 MHz with a drain voltage of 20 V.

EXAMPLE 5

A process which comprises selectively crystallizing an amorphous silicon film by selectively treating the oxide film base using a plasma treatment, and further enhancing the crystallization by irradiating a laser light is described below. The present example comprises a treatment using laser irradiation in addition to the process described in EXAMPLE 2.

Referring to FIG. 8, a 2,000 Å thick silicon oxide film 22 was deposited as a base on a Corning #7059 substrate 21 by sputtering, and a heat-resistant photoresist 24 was applied thereon by spin-coating. After patterning the resulting photoresist film 24, the entire substrate was exposed to nitrogen plasma in the same manner as in Example 1 to perform plasma treatment on the exposed portion 23 of the oxide film base. The plasma treatment was effected under the same conditions as those employed in Example 1, except for setting the RF power to 20 W. Thus was obtained a structure shown in FIG. 8(A).

Since the substrate at this point is heated to a temperature of 200 °C or higher, the masking material to be used herein must at least resist to the same temperature. Furthermore, preferably, the masking material is removable without using a plasma. Thus, the use of a heat-resistant photoresist for the mask is preferred from these points of view. Otherwise, inorganic materials such as titanium nitride, silicon oxide, and silicon nitride can be used as well.

Then, the photoresist 24 was removed.

Subsequently, an annealing at 550 °C for a duration of 4 hours is performed after depositing a 1,500 Å thick amorphous silicon film 25 by reduced pressure CVD. As a result, crystalline silicon 26 was observed to form around the portions remained uncovered by the masking material on plasma treatment. The crystallization extended into portions covered by the masking material (but only portions treated by the plasma) for about 5 μm along the longitudinal direction. No crystallization was observed to occur on other portions 27 covered by the masking material.

After the thermal annealing above, a laser beam 80 was irradiated to the resulting structure. The laser annealing was performed by irradiating 2 shots using a KrF excimer laser operating at a wavelength of 248 nm and a pulse width of 20 nsec, and emitting a laser beam at an energy density of from 200 to 400 mJ/cm^2 . During the laser annealing, the temperature of the substrate was maintained in the temperature range of from 150 to 300 °C, for instance, at 200 °C by heating, to make the best of the effect exerted by laser irradiation.

Other usable laser light include those emitted from a XeC1 excimer laser operating at a wavelength of 308 nm and an ArF excimer laser operating at a wavelength of 193 nm. Otherwise, an intense light may be irradiated in the place of a laser light. In particular, the application of RTA (rapid thermal annealing) which comprises irradiating an infrared light is effective because it can selectively heat the silicon film in a short period of time. A silicon film having a favorable crystallinity

can be obtained by employing any of the aforementioned methods. Thus, the crystallized region 26 obtained as a result of thermal annealing was found to change into a silicon film 26' having a further improved crystallinity. A polycrystalline film 27' was obtained from the region remained uncrystallized 27 as a result of laser irradiation. This film 27', though apparently modified, was confirmed to have poor crystallinity by Raman spectroscopy. Furthermore, observation by transmission electron microscope revealed that numerous minute crystallites constitute the film 27', and that grain-oriented relatively large crystallites constitute the film 26'.

The resulting crystallized silicon film 26' was processed into island-like portions in the same manner as in EXAMPLE 3 (see FIG. 3) to obtain a TFT with considerably improved characteristics. More specifically, an N-channel TFT fabricated using the silicon film obtained in the present example yielded a field-effect mobility in the range of from 150 to 200 cm^2/Vs and a threshold voltage of from 0.5 to 1.5 V, which are in clear contrast with the values obtained on a previously obtained TFT using the silicon film obtained in EXAMPLE 2, namely, a mobility in the range of from 50 to 90 cm^2/Vs and a threshold value of 3 to 8 V. It can be seen that the mobility is greatly increased, and that the fluctuation in the threshold voltage is considerably decreased.

Conventionally, the above improvements in characteristics were only achievable by laser crystallization of the amorphous silicon film. The silicon films which were obtained by a prior art process by laser crystallization, however, had considerable fluctuation in the film characteristics. Moreover, they could not be fabricated by mass production because the crystallization thereof required a temperature of 400 °C or higher and an irradiation of a laser beam at an energy density of 350 mJ/cm^2 or higher. In contrast to a prior art process, the process according to the present example can be performed at a substrate temperature lower than the conventional one and by irradiating a laser beam at a far lower energy density. Furthermore, films of uniform quality can be obtained by the process according to the present invention at a yield well comparable to those fabricated by solid phase growth crystallization according to a conventional thermal annealing process. Thus, the TFTs fabricated therefrom also exhibited uniform characteristics.

It was found in the present invention that, when the concentration of nickel is low, the crystallization of silicon film occurs insufficiently. Accordingly, TFTs with poor characteristics result by using such silicon films. However, the process according to the present example provides a silicon film whose in-

sufficient crystallinity is compensated by the effect of laser irradiation. Accordingly, silicon films containing nickel at a low concentration were also made usable in TFTs by the process of the present example without impairing the characteristics of the resulting TFT. Thus, devices containing less nickel in the active layer region, i.e., those more favorable from the viewpoint of electric stability and reliability, could be implemented.

EXAMPLE 6

The present example provides a process for introducing a catalytic element into the amorphous silicon film by coating the upper surface of the amorphous film with a solution prepared by introducing a catalytic element which accelerates the crystallization.

In the present example, the catalytic element is selectively introduced to allow the crystallites in this region to grow into the portions remained free from the catalytic elements. In this manner, crystalline silicon film can be obtained without increasing the concentration of the catalytic element.

Referring to FIG. 9, a silicon oxide film 902 was deposited on a Corning #7059 substrate 901 (10 cm^2 in size) by sputtering or by plasma CVD. Then, after depositing a 1,000 Å thick amorphous silicon film by plasma CVD, a 500 Å thick silicon oxide film 905 was deposited by sputtering to provide a protective coating. To this structure was dropped 5 ml (for a 10- cm^2 square substrate) of an acetate solution added therein 100 ppm by weight of nickel. A spinner 900 was operated at 50 rpm for a duration of 10 seconds to effect spin coating, thereby forming a uniform aqueous film 907 over the entire surface of the substrate. Furthermore, after maintaining the coated state for 5 minutes, the resulting structure was subjected to 60 seconds of spin drying by operating the spinner 900 at a rate of 2,000 rpm. The retention above may be otherwise conducted by applying a spinner rotating at 150 rpm or lower. Thus is obtained a structure shown in FIG. 9(A).

Subsequently, the amorphous silicon film 904 was crystallized by heating it at 550 °C under a nitrogen atmosphere for a duration of 8 hours. The crystal growth takes place during the heat treatment in such a manner that the crystals grow transversely along a direction indicated with an arrow 916, from a region 906 into which nickel was introduced to a region 903 free from the incorporation of nickel. As a matter of course, crystallization occurs also in the region 904 into which nickel was introduced directly.

Referring to FIG. 9(A), the crystallization occurs on the region 904 into which nickel had been directly introduced, and also on the region 903 in

which the crystallization proceeds along a transverse direction. The concentration distribution for nickel in the region 903 is illustrated in FIG. 10. The distribution curve in FIG. 10 is based on the data of nickel concentration obtained by SIMS (secondary ion mass spectroscopy). It is confirmed that the nickel concentration in the region 904 into which nickel had been directly introduced is about a digit or more higher than the concentration shown in the graph of FIG. 10.

The nickel concentration distribution illustrated in the graph of FIG. 10 can be controlled by controlling the nickel concentration of the solution. In the present invention, the nickel concentration of the solution was adjusted to 100 ppm. However, it is known that crystallization also occurs even if the concentration of the solution is set to 10 ppm. The nickel concentration in the region 903 in FIG. 9 can be further lowered by a digit by setting the nickel concentration of the solution to 10 ppm. However, a problem newly arises by decreasing the nickel concentration of the solution, because the distance 916 of crystal growth along the transverse direction is shortened.

Furthermore, it is also effective to further improve the crystallinity of the crystalline silicon film thus obtained by irradiating a laser beam or an intense light equivalent thereto in the similar manner as in EXAMPLE 5. In the case of Example 5, however, the morphology of the film was impaired because, due to nickel included at a relatively high concentration, nickel precipitated from the silicon film to form grains of nickel silicide from about 0.1 to 10 μm in size in the silicon film. In contrast to the case of EXAMPLE 5 using plasma treatment to incorporate nickel inside the film, the nickel concentration can be far lowered in the present case. Accordingly, no precipitation of nickel silicide is found to form, and surface roughening of the film due to laser irradiation can be prevented from occurring.

The crystalline silicon film thus subjected to crystallization can be used directly in the active layer of a TFT. In particular, the use of the region 903 as the active layer of a TFT is extremely useful because this region contains catalytic elements at a very low concentration.

More specifically, the process for fabricating a TFT using the crystalline silicon film above comprises, as shown in FIG. 9(B) and the subsequent figures, etching the silicon film into an island-like portion to form an island-like silicon region 908. After etching the protective oxide film 905 the resulting structure is subjected to an oxidizing atmosphere in the temperature range of from 500 to 750 $^{\circ}\text{C}$, preferably in the range of from 550 to 650 $^{\circ}\text{C}$, to form a silicon oxide film 909 which functions as a gate insulator film on the surface of the silicon

region. In this step of heat treatment, the oxidizing reaction can be further accelerated by incorporating water vapor, nitrous oxide, and the like into the atmosphere. As a matter of course, a known vapor phase growth process such as plasma CVD and sputtering can be used as an alternative means for forming the silicon oxide film 909, instead of performing the aforementioned thermal oxidation step.

After thus forming an island-like silicon region 908 and a silicon oxide film 909, a connection 910 which functions as a gate contact is formed using a material capable of being anodically oxidized, such as aluminum, is formed in such a manner that it may transverse the island-like silicon region. Preferably, aluminum containing from 0.05 to 0.3 % by weight of scandium is used herein to prevent hill-lock from occurring. Thus, the structure shown in FIG. 9(B) is obtained.

In the same manner as in EXAMPLE 4, the surface of the connection 910 was anodically oxidized to form a 0.1 to 1 μm thick anodically oxidized film 911 on the surface thereof. The resulting structure is shown in FIG. 9(C).

Then, an impurity was introduced into the structure using plasma doping. In this case, phosphine (PH_3) gas was used as the doping gas. Phosphine was doped at an accelerating voltage of 80 keV, and the thus doped impurity was activated by further laser annealing the structure applying 5 shots of laser using a KrF excimer laser operating at a wavelength of 248 nm and emitting a laser beam at an energy density of from 250 to 300 mJ/cm^2 . Thus were formed the impurity regions 912 and 913. In this case, the gate contact is offset from the impurity region by a distance corresponding to the thickness x of the anodic oxide. The resulting structure is shown in FIG. 9(D).

Finally, a 5,000 \AA thick silicon oxide film was deposited as an interlayer insulator 914 in the same manner as in an ordinary process for fabricating a TFT. Additionally, a light-transmitting polyimide film 915 was formed by spin coating to form a further smoother surface. By forming contact holes in the resulting film, connection and contacts 917 and 918 were formed in the source region and the drain region. Thus was obtained the final structure of the TFT as shown in FIG. 9(E).

In the present example, an acetate solution was used as the solution containing the catalytic element. However, an aqueous solution, a solution based on an organic solvent, etc., which is selected from a wide variety, can be used as well. The catalytic element may not be included in the solution as a compound, and it may be simply dispersed in the solution.

The catalytic element can be incorporated into a solvent selected from polar solvents, for example, water, an alcohol, an acid, and ammonia.

When nickel is selected as the catalytic element, nickel is incorporated into a polar solvent by using a nickel compound. The nickel compounds to be used for this purpose include, representatively, nickel bromide, nickel acetate, nickel oxalate, nickel carbonate, nickel chloride, nickel iodide, nickel nitrate, nickel sulfate, nickel formate, nickel acetylacetate, nickel 4-cyclohexylbutyrate, nickel oxide, and nickel hydroxide.

Solvents to be used in the present invention include a non-polar solvent such as benzene, toluene, xylene, carbon tetrachloride, chloroform, and ethers.

In using a solvent, nickel is introduced in the form of a nickel compound. The nickel compounds to be used for this purpose include nickel acetylacetate and nickel 2-ethylhexanate.

It is also useful to incorporate a surfactant in the solution containing the catalytic element. The incorporation increases the adhesion strength of the solution to the coating surface and controls the adsorptivity. Otherwise, the surfactant may be previously applied to the surface to be coated with the solution. When metallic nickel is used as the catalytic element, it must be previously dissolved in an acid to use it in the form of a solution thereof.

The foregoing cases refer to examples using a solution into which the catalytic element, nickel, is completely dissolved. Nickel need not be completely dissolved in the solution, and materials in an other form, for instance, an emulsion comprising a powder of metallic nickel or a powder of a compound of nickel uniformly dispersed in a dispersion medium can be used as well.

The aforementioned facts also apply to any material using a catalytic element other than nickel.

A non-polar solution such as a toluene solution of nickel 2-ethylhexanate can be directly applied to the surface of an amorphous silicon film. In this case, it is also effective to previously coat the amorphous silicon film with an adhesive generally used in coating a resist. However, the use thereof must be done carefully, because the application thereof in too large an amount reversely interferes the addition of the catalytic element into the amorphous silicon film.

The catalytic element is incorporated into the solution approximately in an amount of, though depending on the type of the solution, from 1 to 200 ppm by weight, and preferably, from 1 to 50 ppm by weight. This range of addition is determined by taking the nickel concentration of the crystallized film and the resistance against hydrofluoric acid into consideration.

As described in the foregoing, the present invention is epoch-making in that it enables the crystallization of an amorphous silicon to take place at an even lower temperature and within a shorter

period of time. Furthermore, the process according to the present invention is suitable for mass production, and yet, it can be performed employing the most commonly used equipments, apparatuses, and methods. Accordingly, it is a promising and a beneficial process for the electronic industry.

More specifically, for instance, a conventional solid phase growth process requires an annealing step for a duration of at least 24 hours. Considering that the process time per substrate is preferably 2 minutes, 15 annealing furnaces are necessary to make the process practically feasible. However, the present invention allows the process to complete within 8 hours, and under optimal conditions, the process can be even more shortened to a mere 4 hours or less. This signifies that the process can be performed while reducing the number of furnaces to only a sixth or less of the above calculated number. This leads to an increase of productivity and the cutting down of equipment investment, thereby lowering the process cost of the substrates. Accordingly, economical TFTs can be produced, and this might call novel demands. Conclusively, the present invention is greatly beneficial for the industry.

While the invention has been described in detail and with reference to specific embodiments thereof, it will be apparent to one skilled in the art that various changes and modifications can be made therein without departing from the spirit and scope thereof.

Claims

1. A process for fabricating a semiconductor comprising the steps of:

forming an insulator coating on a substrate;

exposing said insulator coating to a plasma;

forming an amorphous silicon film on said insulator coating after said exposing step; and crystallizing said silicon film by photo annealing said silicon film and/or heat treating said silicon film in the temperature range of from 400 to 650 °C.

2. The process of claim 1 wherein the substrate is heated in a temperature range of from 100 to 500 °C during said exposing step.

3. The process of claim 1 wherein the plasma comprises 10 % by volume or more of at least one selected from the group consisting of nitrogen, oxygen, neon, krypton, and argon.

4. The process of claim 1 wherein said substrate is not exposed to air between said exposing step and said amorphous silicon film forming step.
5. The process of claim 1 wherein said exposing step is carried out in a space provided therein an electrode made of a material containing at least one element selected from a group consisting of nickel, iron, cobalt, and platinum.
6. The process of claim 1 further comprising a step of irradiating a laser beam or an intense light equivalent to a laser beam to said silicon film after said heat treating step.
7. The process of claim 3 wherein the plasma further comprises a gas selected from the group consisting of hydrogen and helium as a dilution gas.
8. A process for fabricating a semiconductor comprising the steps of:
 - forming an insulator coating on a substrate;
 - selectively coating said insulator coating with a masking material;
 - exposing said substrate to a plasma;
 - forming an amorphous silicon film on said insulator coating after said exposing step;
 - crystallizing said silicon film by photo annealing said silicon film and/or heat treating said silicon film in the temperature range of from 400 to 650 °C; and
 - selectively etching said silicon film.
9. The process of claim 8 wherein the substrate is heated in a temperature range of from 100 to 500 °C during said exposing step.
10. The process of claim 8 wherein the plasma comprises 10 % by volume or more of at least one selected from the group consisting of nitrogen, oxygen, neon, krypton, and argon.
11. The process of claim 10 wherein the plasma further comprises a gas selected from the group consisting of hydrogen and helium as a dilution gas.
12. A process for fabricating a thin film transistor comprising the steps of:
 - forming an insulator coating on a substrate;
 - selectively coating said insulator coating with a masking material;
 - exposing said substrate to a plasma;
 - forming an amorphous silicon film on said

insulator coating after said exposing step;

crystallizing said silicon film by photo annealing said silicon film and/or heat treating said silicon film in the temperature range of from 400 to 650 °C;

selectively etching said silicon film; and
 establishing a channel forming region of the thin film transistor on the portion previously coated with the masking material.

13. The process of claim 12 wherein the plasma comprises 10 % by volume or more of at least one selected from the group consisting of nitrogen, oxygen, neon, krypton, and argon.
14. The process of claim 13 wherein the plasma further comprises a gas selected from the group consisting of hydrogen and helium as a dilution gas.
15. A process for fabricating a semiconductor comprising the steps of:
 - forming an amorphous silicon film on a substrate;
 - forming, in intimate contact with the upper or the lower surface of said silicon film, a substance comprising an element which accelerates the crystallization of amorphous silicon by exerting a catalytic effect thereto; and
 - crystallizing said silicon film by photo annealing said silicon film and/or heating said silicon film at a temperature of 400 °C or higher, but not higher than the glass transition temperature of the substrate.
16. A process for fabricating a semiconductor comprising the steps of:
 - forming an insulator coating on a substrate;
 - forming a layer comprising an element selected from the group consisting of nickel, iron, cobalt, and platinum on said insulator coating;
 - forming a silicon film in contact with said layer before or after said layer forming step; and
 - crystallizing said silicon film by photo annealing said silicon film and/or heating said silicon film.
17. The process of claim 16 wherein said layer has a form selected from the group consisting of atom, island, cluster and film.
18. A process for fabricating a semiconductor comprising the steps of:
 - forming a liquid layer comprising an element selected from the group consisting of nickel, iron, cobalt and platinum on a substrate

by spin coating;
forming a silicon film on said substrate;
and
crystallizing said silicon film with said element being incorporated into said silicon film by photo annealing and/or heating said silicon film.

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19. A process for fabricating a semiconductor comprising the steps of:

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forming an insulator coating on a substrate;

selectively coating said insulator coating with a masking material;

coating on the surface of the substrate, a substance containing an element which accelerates the crystallization of amorphous silicon by exerting a catalytic effect thereto;

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forming an amorphous silicon film on said insulator coating after said substance coating step;

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crystallizing said silicon film by photo annealing said silicon film and/or heat treating said silicon film in the temperature range of from 400 to 650 °C; and

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selectively etching said silicon film.

20. A process for fabricating a semiconductor comprising the steps of:

forming an amorphous silicon film on a glass substrate;

30

selectively coating said silicon film with a masking material after said amorphous silicon film forming step;

coating on the surface of the substrate, a substance containing an element which accelerates the crystallization of amorphous silicon by exerting a catalytic effect thereto;

35

crystallizing said silicon film by photo annealing said silicon film and/or heat treating said silicon film at a temperature of 400 °C or higher, but not higher than the glass transition temperature of the substrate; and

40

selectively etching said silicon film.

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FIG. 1

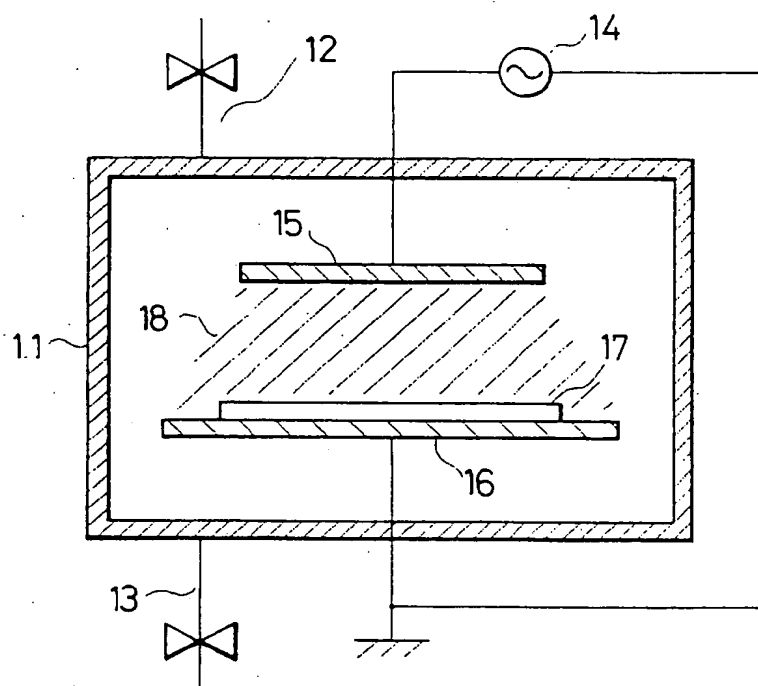


FIG. 2(A)

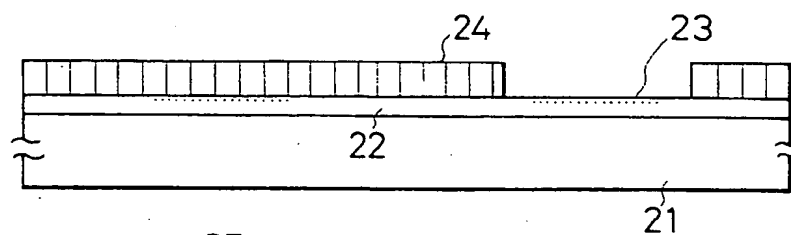


FIG. 2(B)

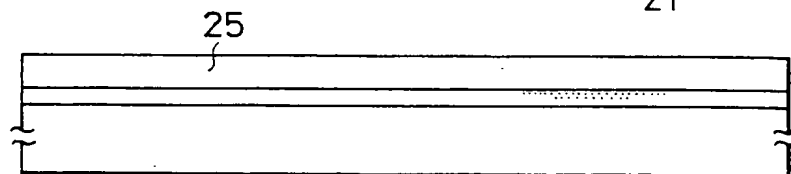


FIG. 2(C)

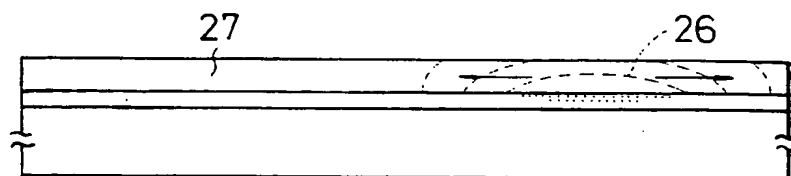


FIG. 3(A)

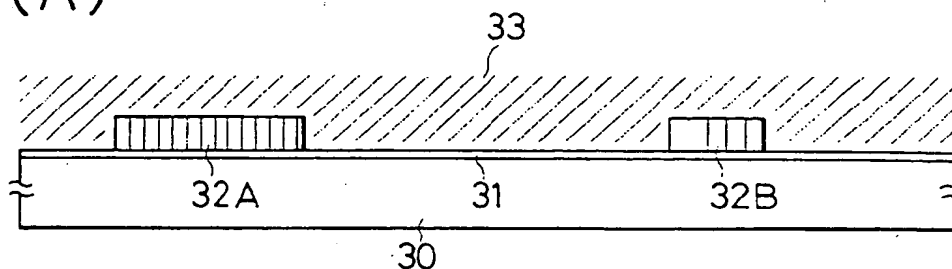


FIG. 3(B)

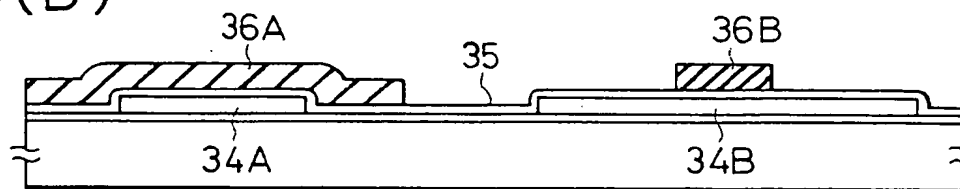


FIG. 3(C)

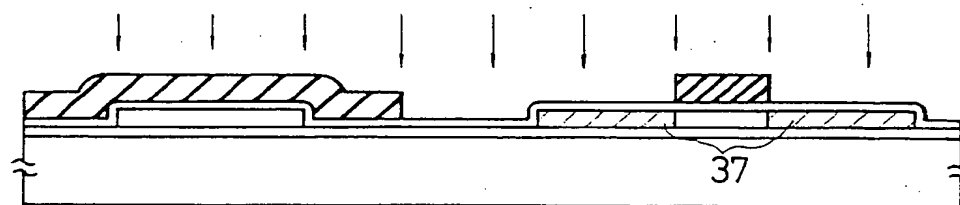


FIG. 3(D)

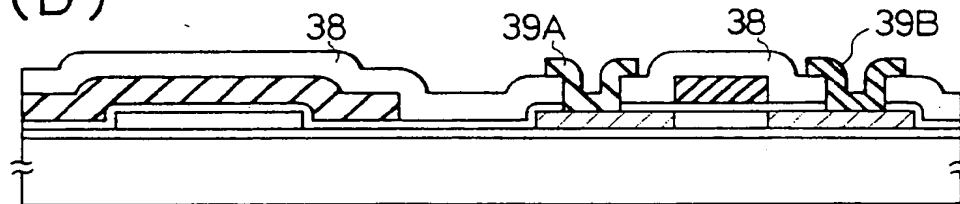


FIG. 3(E)

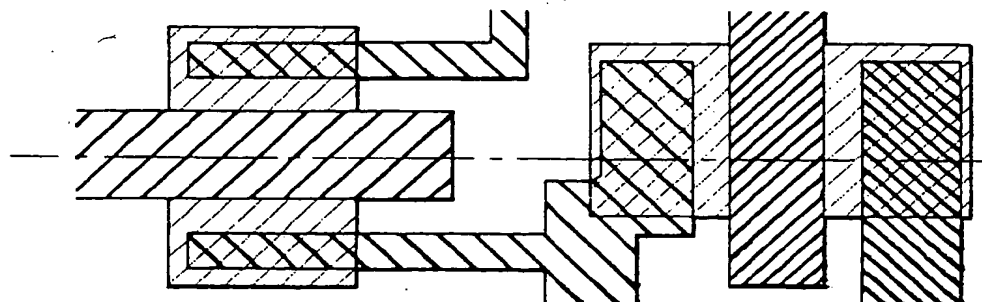


FIG. 4(A)

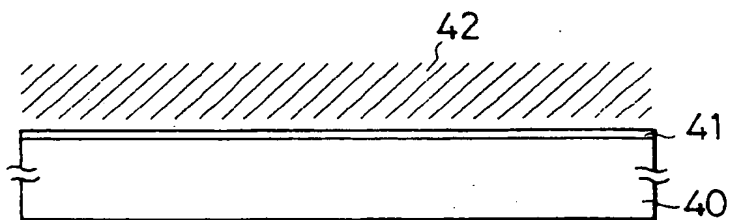


FIG. 4(B)

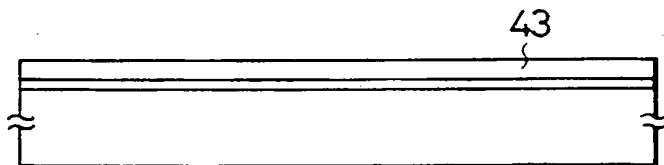


FIG. 4(C)

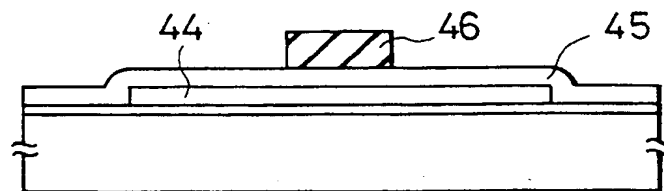


FIG. 4(D)

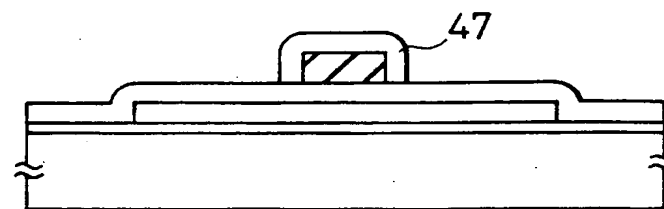


FIG. 4(E)

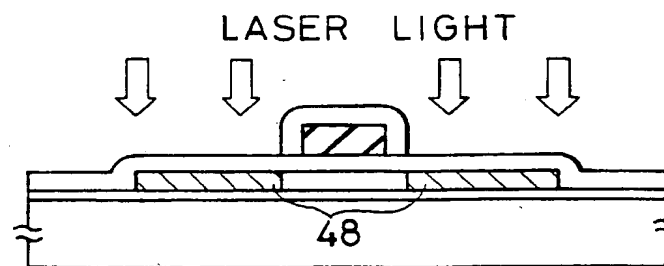


FIG. 4(F)

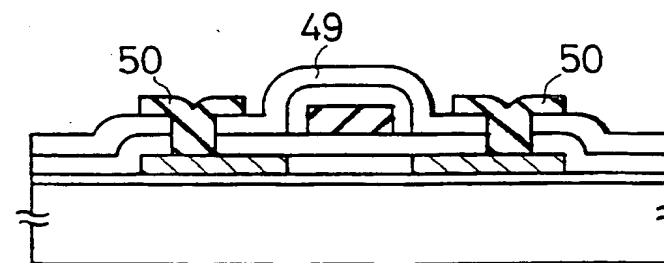


FIG. 5

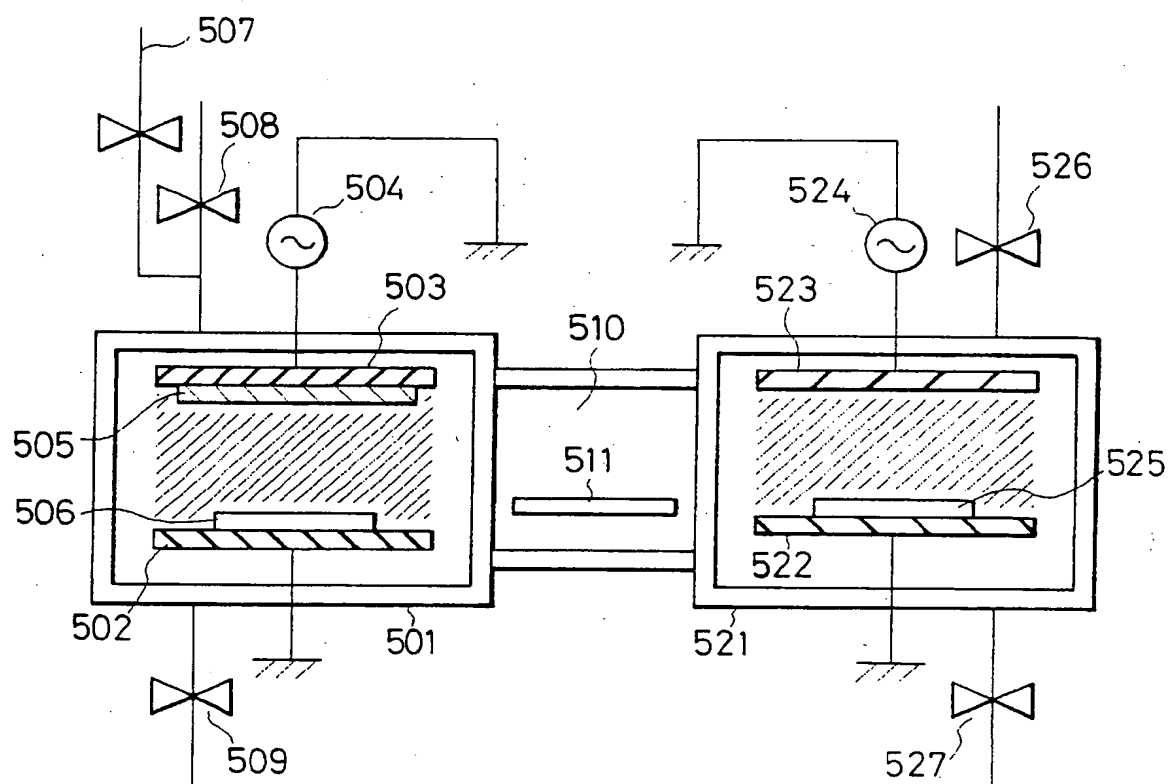


FIG. 6

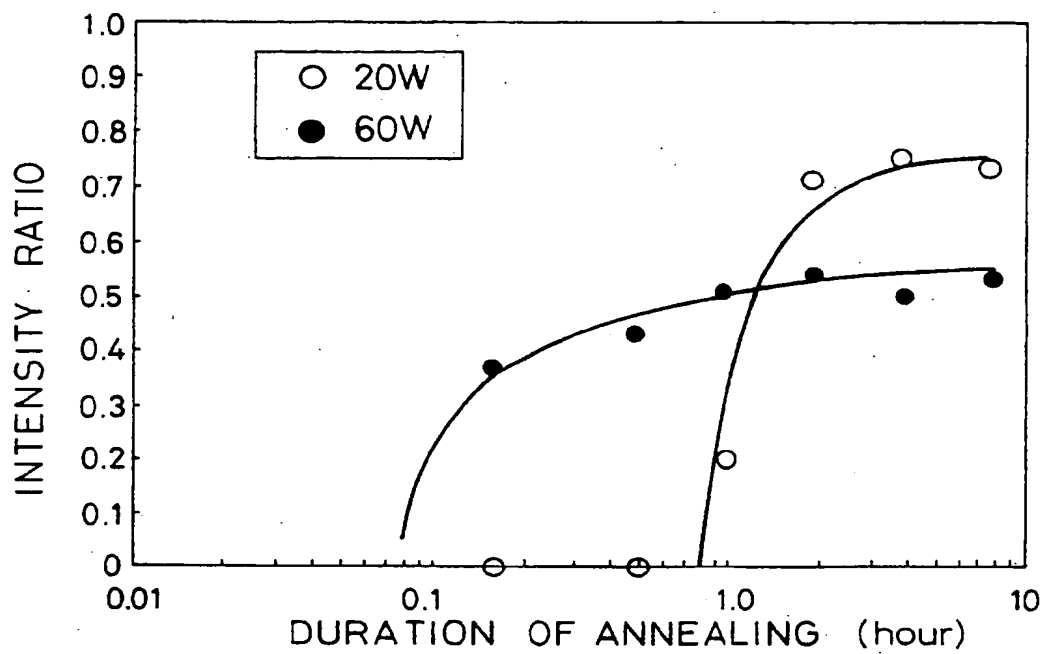


FIG. 7

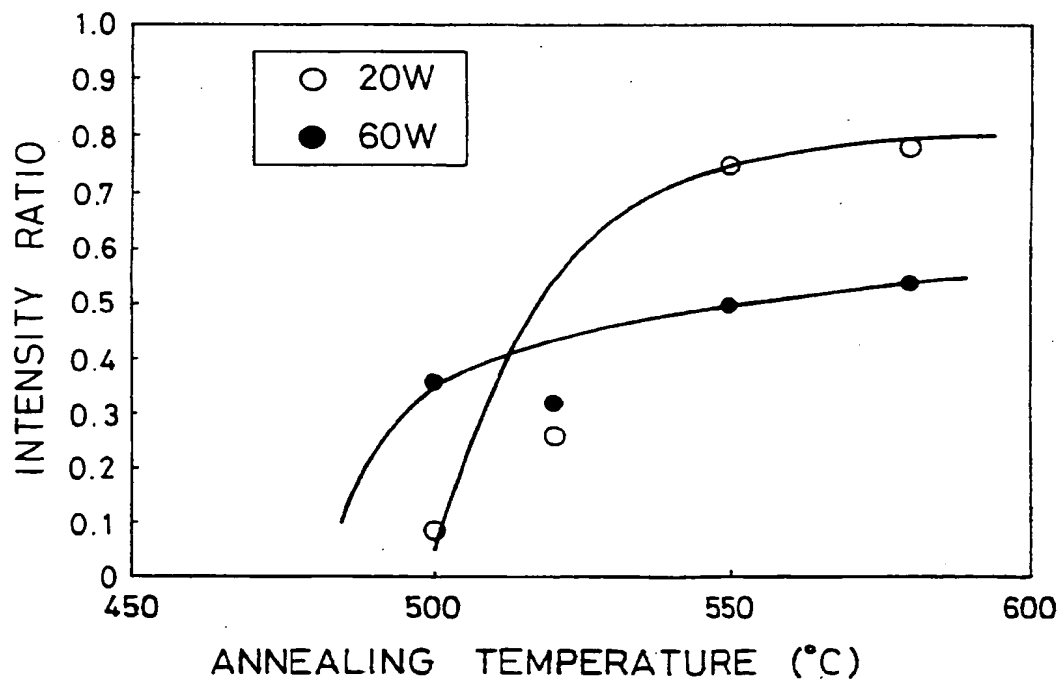


FIG.8(A)

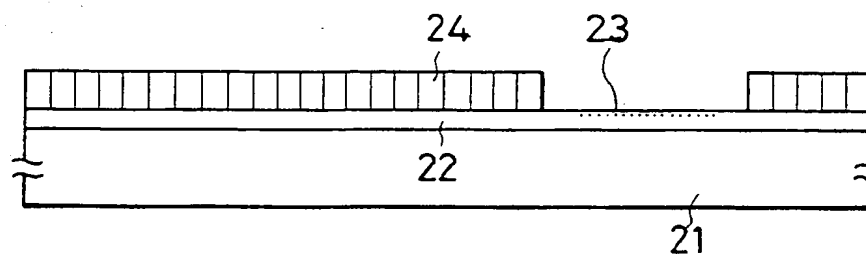


FIG.8(B)

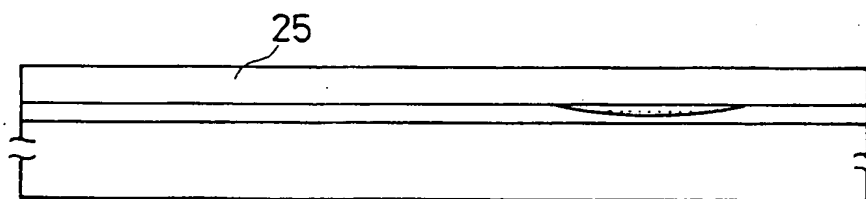


FIG.8(C)

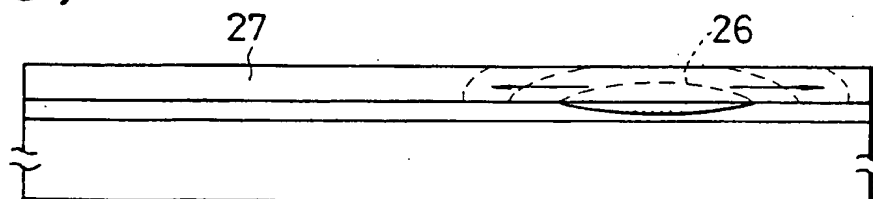


FIG.8(D)

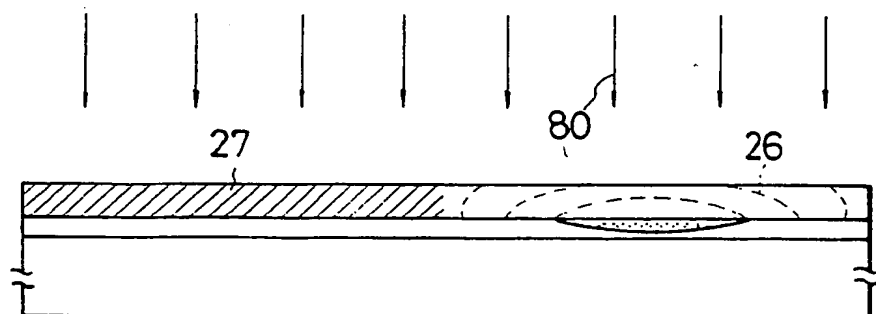


FIG. 9(A)

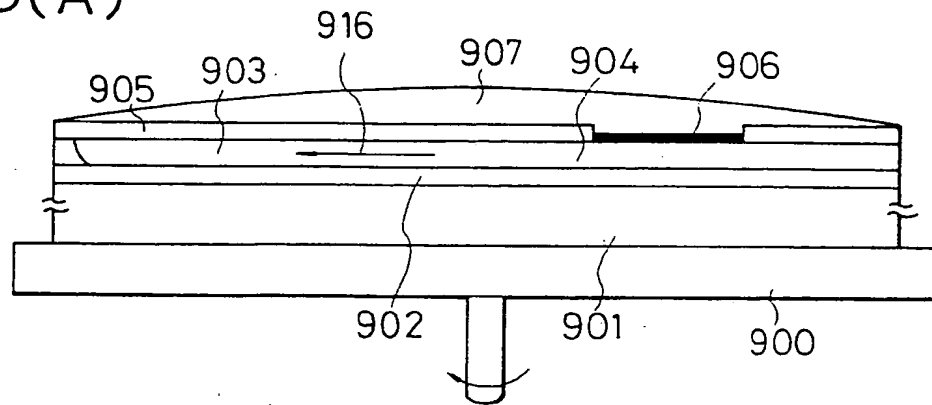


FIG. 9(B)

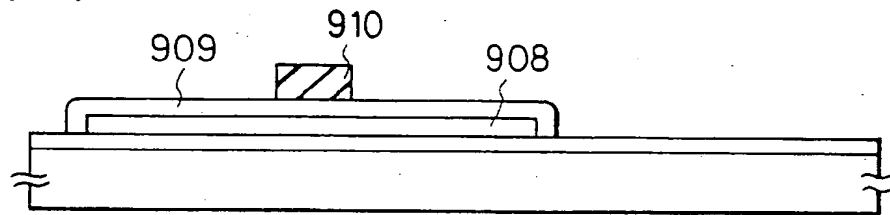


FIG. 9(C)

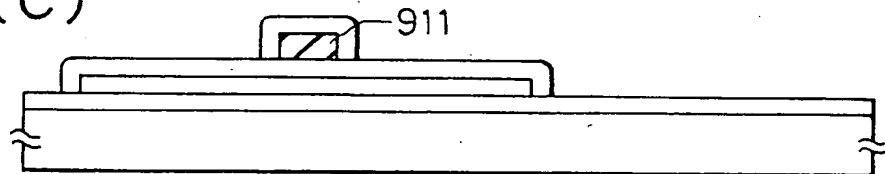


FIG. 9(D)

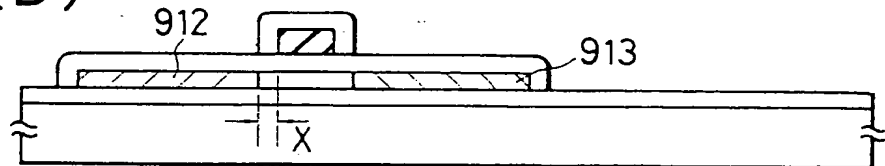


FIG. 9(E)

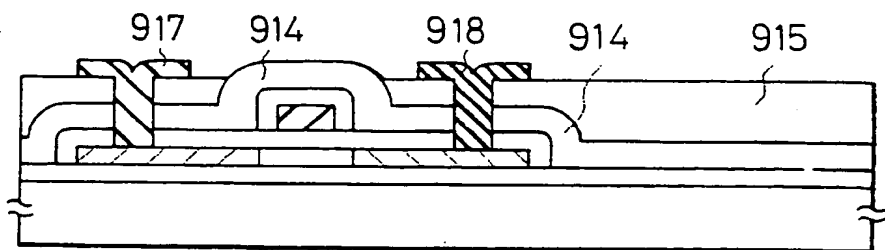
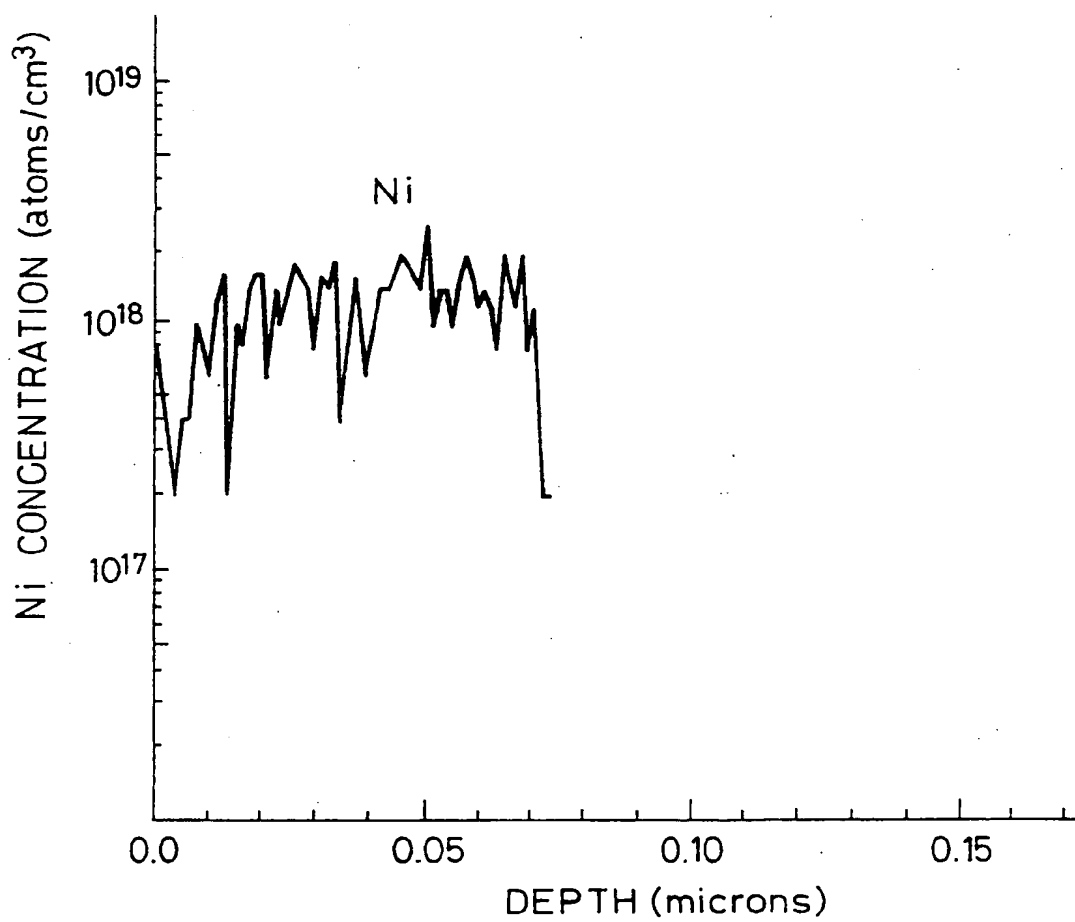


FIG. 10



(19)



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(11) Publication number:

0 609 867 A3

(12)

EUROPEAN PATENT APPLICATION(21) Application number: **94101571.1**(51) Int. Cl.⁶: **H01L 21/20, H01L 21/336**(22) Date of filing: **02.02.94**(30) Priority: **03.02.93 JP 39499/93**(43) Date of publication of application:
10.08.94 Bulletin 94/32(84) Designated Contracting States:
DE FR GB NL(88) Date of deferred publication of the search report:
11.01.95 Bulletin 95/02

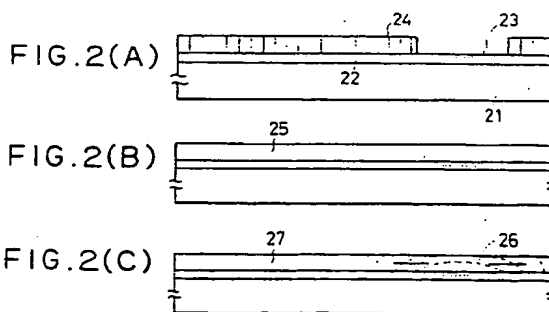
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(54) **Process for fabricating a semiconductor crystallized layer and process for fabricating a semiconductor device using the same.**

(57) A process for fabricating a semiconductor at a lower crystallization temperature and yet at a shorter period of time, which comprises forming an insulator coating on a substrate; exposing said insulator coating to a plasma; forming an amorphous silicon film on said insulator coating after its exposure to said plasma; and heat treating said silicon film in the temperature range of from 400 to 650 °C or at a temperature not higher than the glass transition temperature of the substrate. The nucleation sites are controlled by selectively exposing the amorphous silicon film to a plasma or by selectively applying a substance containing elements having a catalytic effect thereto. A process for fabricating a thin film transistor using the same is also disclosed.

**EP 0 609 867 A3**



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EUROPEAN SEARCH REPORT

Application Number
EP 94 10 1571

DOCUMENTS CONSIDERED TO BE RELEVANT			
Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.5)
A	PATENT ABSTRACTS OF JAPAN vol. 16, no. 59 (E-116) 14 February 1992 & JP-A-03 257 818 (SEIKO EPSON CORP) 18 November 1991 * abstract *	1,12	H01L21/20 H01L21/336
A	EP-A-0 421 605 (CANON K.K.) * column 3, line 43 - column 4, line 24 * * example 1 *	1,3,4	
A	PATENT ABSTRACTS OF JAPAN vol. 16, no. 271 (E-1218) 18 June 1992 & JP-A-04 062 976 (NIPPON SEIKI CO. LTD) 27 February 1992 * abstract *	6	
X	US-A-5 147 826 (THE PENNSYLVANIA RESEARCH CORPORATION) * column 4, line 4 - line 64 * * example 2 *	15-17,20	
X	WO-A-92 01089 (GEC-MARCONI LIMITED) * page 1, paragraph 2 * * claims 1,3,4 *	15,17	TECHNICAL FIELDS SEARCHED (Int.Cl.5) H01L
A		16,19	
A	THIN SOLID FILMS., vol.47, no.3, December 1977, LAUSANNE CH pages 313 - 321 S.S.LAU ET AL. 'SOLID PHASE EPITAXY IN SILICIDE-FORMING SYSTEMS' *ABSTRACT*	16,18	
The present search report has been drawn up for all claims			
Place of search THE HAGUE		Date of completion of the search 14 November 1994	Examiner Schuermans, N
CATEGORY OF CITED DOCUMENTS			
X : particularly relevant if taken alone Y : particularly relevant if combined with another document of the same category A : technological background O : non-written disclosure P : intermediate document		T : theory or principle underlying the invention E : earlier patent document, but published on, or after the filing date D : document cited in the application L : document cited for other reasons & : member of the same patent family, corresponding document	

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EP 94101571.1

CLAIMS INCURRING FEES

The present European patent application comprised at the time of filing more than ten claims.

- ☐ All claims fees have been paid within the prescribed time limit. The present European search report has been drawn up for all claims.
- ☐ Only part of the claims fees have been paid within the prescribed time limit. The present European search report has been drawn up for the first ten claims and for those claims for which claims fees have been paid, namely claims:
- ☐ No claims fees have been paid within the prescribed time limit. The present European search report has been drawn up for the first ten claims.

LACK OF UNITY OF INVENTION

The Search Division considers that the present European patent application does not comply with the requirement of unity of invention and relates to several inventions or groups of inventions, namely:

See Sheet B.

- ☒ All further search fees have been paid within the fixed time limit. The present European search report has been drawn up for all claims.
- ☐ Only part of the further search fees have been paid within the fixed time limit. The present European search report has been drawn up for those parts of the European patent application which relate to the inventions in respect of which search fees have been paid, namely claims:
- ☐ None of the further search fees has been paid within the fixed time limit. The present European search report has been drawn up for those parts of the European patent application which relate to the invention first mentioned in the claims, namely claims:



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EP 94101571.1 - 8 -

LACK OF UNITY OF INVENTION

The Search Division considers that the present European patent application does not comply with the requirement of unity of invention and relates to several inventions or groups of inventions, namely:

1. Claims 1-14: Pretreatment of an insulating substrate with a plasma to improve the crystallisation of A-Si deposited on it and device obtained.
2. Claims 15-20: Crystallisation of an A-Si layer improved by contact of this layer with a catalytic material.

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